IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A system for inspecting electrical circuits comprising:

a boundary identifier operative to generate a representation of boundaries of elements in an image of an electrical circuit which is under inspection; and

a defect identifier operative to receive said representation of boundaries of elements and to analyze at least some locations of at least some boundaries in said representation of boundaries of elements with reference to a corresponding region of acceptable locations to identify defects in said electrical circuit.

2. (original) A system according to claim 1, and wherein said boundary identifier is operative in hardware.

3. (original) A system according to claim 1, and wherein said defect identifier is operative in software.

4. (original) A system according to claim 2, and wherein said defect identifier is operative in software.

5. (original) A system according to claim 1, and wherein said defect identifier is operative to compare an actual location of at least one boundary from among said boundaries in said image under inspection, to a location of a corresponding boundary in at least one reference image.

6. (original) A system according to claim 1, wherein said boundaries comprise contours.

7. (original) A system according to claim 1, and wherein said system further includes a putative defect detector operative to identify at least some putative defects.

8. (original) A system according to claim 7, and wherein said defect identifier is operative to analyze, from among said at least some boundaries, those boundaries that are associated with said putative defects.

9. (original) A system according to claim 1, and wherein said system farther includes a region of interest identifier operative to identify a portion of said image of an electrical circuit as being a region of interest.

10. (original) A system according to claim 9, and wherein said defect identifier is operative to analyze, from among at least some boundaries, only those boundaries that are in said region of interest.

11. (original) A system according to claim 8, and wherein said system further includes a region of interest identifier operative to identify a portion of said image of an electrical circuit as being a region of interest, and said defect identifier is operative to analyze at least one characteristic of said at least some boundaries that are in said region of interest.

12. (currently amended) A method for inspecting electrical circuits comprising:

generating a representation of boundaries of elements in an image of an electrical circuit; and

analyzing at least one of said boundaries in said representation of boundaries of elements with reference to a corresponding region of acceptable locations to identify defects in said electrical circuit.

13. (original) A method according to claim 12, and wherein said generating is performed in hardware.

14. (original) A method according to claim 12, and wherein said analyzing is performed in software.

15. (original) A method according to claim 13, and wherein said analyzing is performed in software.

16. (original) A method according to claim 12, and wherein said analyzing comprises analyzing at least one characteristic of a location of at least some of said boundaries.

17. (original) A method according to claim 16, and wherein said analyzing a location of at least some of said boundaries comprises comparing at least one characteristic of a location of a selected boundary to at least one characteristic of a location of a corresponding boundary in a reference.

18. (original) A method according to claim 12, and further including identifying a portion of said image of an electrical circuit as being a region of interest.

19. (canceled)

20. (currently amended) A ~~system~~ method according to claim ~~19~~12, wherein said corresponding region of acceptable locations ~~threshold vicinity~~ comprises an envelope around the at least one boundary in the at least one reference image.

21. (currently amended) A method of manufacturing an electrical circuit comprising:

acquiring an image of at least a portion of an electrical circuit and inspecting said image for defects in said electrical circuit, said inspecting including: generating a representation of boundaries of elements in the image; and

analyzing at least one of said boundaries in said representation of boundaries of elements with reference to a corresponding region of acceptable locations to identify defects in said electrical circuit portion.

22. (original) A method according to claim 21, and wherein said generating is performed in hardware.

23. (original) A method according to claim 21, and wherein said analyzing is performed in software.

24. (original) A method according to claim 22, and wherein said analyzing is performed in software.

25. (original) A method according to claim 21, and wherein said analyzing comprises analyzing at least one characteristic of a location of at least some of said boundaries.

26. (original) A method according to claim 25, and wherein said analyzing a location of at least some of said boundaries comprises comparing at least one characteristic of a location of a selected boundary to at least one characteristic of a location of a corresponding boundary in a reference.

27. (original) A method according to claim 21, and further including identifying a portion of said image of an electrical circuit as being a region of interest.